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Electroless Deposition

Liquid-Phase Deposition of Freestanding Copper Foils and Supported Copper Thin Films and Their Structuring into Conducting Line Patterns**

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Copper plays a fundamental role in electronics. The low bulk electrical resistivity, high thermal conductivity, good machining and joining properties, and high availability lead to the situation that more than 60% of all copper is processed in the electrical industry. Inventions such as the telegraph, telephone, and radio around 1900 laid the foundation for the origin of the printed circuit board (PCB) with copper as trace material.[1] In the 1960s, the PCB itself inspired the creation of the integrated circuit (IC), and it was in the 1990s when the breakthrough of copper as interconnecting material hit the microelectronic research and development community.[1,2] The preferential usage of copper as trace and interconnecting material in microelectronics is primarily based on its high bulk electrical conductivity and higher resistance against electromigration compared to the alternative material aluminum.[2–8]

The rapidly advancing reduction of the feature size of electronic devices makes it necessary to scale down the conducting copper traces and copper lines. Latest achievements even describe the preparation of conducting nanocables as connectors in nanodevices.[9] But depending on the degree of line width or foil thickness confinement, electron scattering effects lead to an unwanted increase in the electrical resistivity.[10–12] Major contributions to the hindrance of the electron flow arise from inelastic grain boundary, surface/interface and surface roughness scattering of electrons. Additionally, electromigration becomes a reliability issue.[1] Fast atomic diffusion pathways, such as surfaces/interfaces or grain boundaries, facilitate the movement of copper ions driven by the momentum transfer from the electrons leading to void/hillock formation and track thinning, ending in open-circuit failure.[13,14] Because the electrical resistivity is proportional to the grain boundary area per unit volume and high diffusivity grain boundaries (especially grain boundary triple points) favor electromigration phenomena, a bamboo-like microstructure would ideally counteract the problem of increasing resistivity and device failure owing to electromigration. However, control over the microstructure is difficult to achieve with the current technology. As it is today, the manufacturing technology applied in combination with the geometric size predefines the microstructure of the resulting copper interconnect/trace or copper foil to a great degree.

The conventional deposition processes can roughly be categorized into physical vapor deposition (PVD), chemical vapor deposition (CVD), electroplating (EP), and electroless deposition techniques.[6,15–19] In the damascene process for modern ICs, the copper interconnects are prepared by depositing a copper thin film on a patterned surface. Besides its structural stability, the most important requirement is a void free and conformal deposition of the copper thin film,[19–23] which is achieved by electroplating the interconnecting copper on top of a seed layer. The copper seed layer, deposited by CVD, PVD, or electroless techniques, is essential for the nucleation and growth of the electroplated copper. A full coverage of the underlying barrier layer by the seed layer is necessary to prevent any void formation in the acidic plating bath. Most of the techniques used in the damascene process are however no longer suitable to meet the needs of future ICs.[1] For example, although PVD in general is a versatile technique to deposit uniform and isotropic thin films over steps edges and lines, it fails in filling high aspect ratio (depth/width) features owing to low sidewall coverage.[24] CVD processes suffer from other problems, such as expensive precursors and/or slow deposition speed, which prevent the formation of thicker films. In comparison to these two techniques, electroplating does not require cost intensive high vacuum chambers. Electroplated copper traces or thin films suffer however from recrystallization phenomena at room temperature, which drastically change their microstructure and reliability.[25,26] To control the electroplating process different additives are included in the bath, which in the end increase the electrical resistivity owing to the presence of impurity atoms and second-phase particles.[27,28] Accordingly, electroless plating seems to be an interesting alternative for the deposition of copper thin films. However, subtle control over the deposition process is challenging, and the grain size of electroless plated copper films is typically too small, offering many scattering sites for electrons and diffusion pathways for electromigrating copper ions.

The present work outlines a novel and profoundly simple electroless, non-aqueous deposition technique that is appli-

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cable to the preparation of freestanding submicrometer-thin copper foils as well as to copper-supported thin films, for example on flexible substrates such as Kapton. Both configurations are highly relevant from a technological point of view. The use of copper foils with minimized thickness is required to reduce the amount of undercutting during etching of fine-line designs on high-density printed circuits, whereas the copper plated Kapton allows the preparation of mechanically and thermally stable flexible circuits.

Compared to PVD and CVD deposition techniques, the described process does not need a vacuum chamber or expensive precursor materials. In contrast to electroplating processes, no conducting surface to nucleate the film is needed and the resulting copper structure does not suffer from room-temperature recrystallization phenomena. Furthermore, no impurity atoms and secondary phase particles (catalysts) are present in the bath, which would influence the conduction behavior of the resulting copper thin film. Although the characteristics of the freestanding foils are promising for the laminate manufacturing of high-density printed circuits, herein we decided to outline the high potential of the deposition technique for application in flexible electronics. The Kapton-deposited film was structured forming a conduction line pattern on top of the flexible substrate. In all of the conducted experiments, anhydrous benzyl alcohol (BnOH) serves as solvent and copper(II) acetylacetonate ($Cu(acac)_2$) as precursor. The as-synthesized copper foils and films exhibit low electrical resistivity, a smooth surface, and dense microstructure without any kind of postsynthetic heat treatment, making them perfect candidates for high-density or flexible printed circuit applications.

The experimental details for the preparation of the freestanding copper foil and for the copper plated Kapton foil including the structuring into the conducting line patterns are given in the Supporting Information.

Freestanding copper foil: $Cu(acac)_2$ only dissolves moderately in BnOH at room temperature. Nevertheless, 5 min after heating the reaction solution in a glass vial in a preheated oil bath, the solution turns dark blue to black (Figure 1 A, 5 min). After 24 h, the deposition of Cu_2O at the wall of the vessel leads to the appearance of a reddish to brownish color (Figure 1 A, 24 h). Continued heating at 140 °C results in the slow reduction of copper oxide to metallic copper and finally in the deposition of a shiny copper mirror on the glass wall (Figure 1 A, 50 h). Between 50 and 60 h of reaction, delamination of the copper foil from the glass wall occurs (Figure 1 A, 60 h), producing a freestanding foil floating in the reaction solution. After thoroughly washing with absolute ethanol, pieces of foils in the size range of a few centimeters (Figure 2 A) are obtained. All of the characterization was performed on the as-synthesized copper foil without any further heat treatment.

The X-ray diffraction (XRD) patterns of the compounds extracted after different reaction times (Figure 1 B) give a clear indication about the chemical reaction pathway. The pattern after 24 h matches that of Cu_2O. Between 40 and 50 h, the composition is a mixture between Cu_2O and metallic Cu. After 60 h, the XRD pattern corresponds to pure metallic copper. The same is true for the XRD pattern of the foil, which perfectly fits the reference data of metallic copper (ICDD No. 01-071-4610).

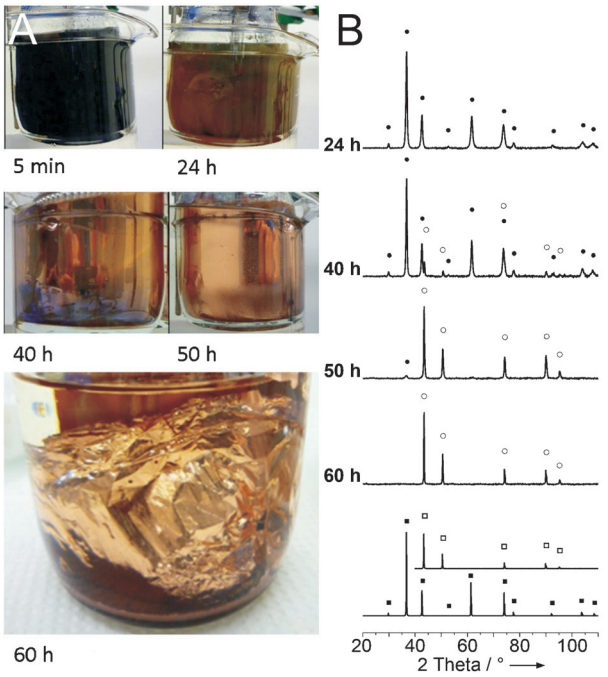

Figure 1. A) Pictures of the glass vials after different reaction times. B) XRD patterns of the compounds obtained after different reaction times: ● Cu_2O, ■ Cu_2O, ICDD No. 00-005-0667, ○ Cu, □ Cu, ICDD No. 01-071-4610.

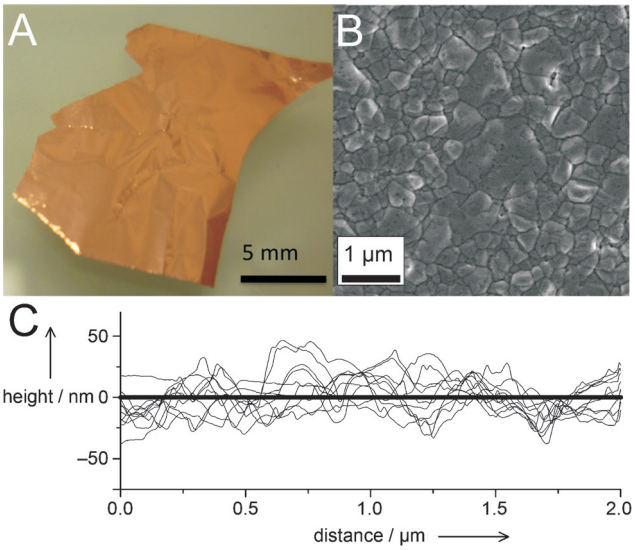

Figure 2. A) The freestanding copper foil. B) SEM micrograph of the copper foil surface showing a dense microstructure with a broad grain size distribution. C) AFM surface profile lines measured across the copper foil surface.

As the shiny appearance of the foil already indicates (Figure 2 A), a root-mean-square (RMS) value of 15.03 ± 2.19 nm obtained from atomic force microscopy (AFM) measurements confirms the low surface roughness of the

copper foil (Figure 2C). Scanning electron microscopy (SEM) investigations of a piece of a copper foil reveal a dense microstructure with a broad grain size distribution (Figure 2B). The grains form a surprisingly strong interconnection, considering the low synthesis temperature of only 140 °C. This observation is confirmed macroscopically, because the foil is stable enough to be handled with tweezers without falling apart. The dense microstructure, high purity, and crystallinity of the copper foil have a positive effect on the electrical properties. Without any additional heat treatment, the as-synthesized foil with a thickness of 500 ± 50 nm shows a low electrical resistivity of 2.2 ± 0.2 μΩ cm, which is comparable to bulk Cu (1.68 μΩ cm).

Conduction line pattern on Kapton foil: The preparation of the conduction line pattern on the Kapton foil involves five steps as schematically shown in the Supporting Information, Figure S1. The experimental results are displayed in Figure 3. Starting from a Kapton foil as substrate (Figure 3, step 1), immersion in the initial reaction solution followed by heating

Figure 3. Pictures of the different substrates during the five-step processing of the copper line pattern from a copper-plated Kapton foil: 1) Uncoated Kapton substrate; 2) substrate after deposition of copper; 3) substrate after deposition of the laser-printed toner pattern onto the copper surface; 4) substrate after etching off the unprotected copper; 5) substrate after removal of the toner by washing with acetone, leaving behind the copper line pattern.

at 140 °C leads to the deposition of a copper layer on the Kapton foil (Figure 3, step 2). SEM micrographs taken from the metal surface (Supporting Information, Figure S2) indicate that the metal film is homogenous, dense, and shows a microstructure that is comparable to that of the freestanding copper foil. The grains exhibit remarkably large dimensions (around 400 nm) compared to those of conventionally electroless deposited copper (around 50 nm).[29–31] This feature is a major advantage with respect to the electrical properties, especially considering that these large grain sizes are obtained without postsynthetic annealing. In the next step, the copper thin film is decorated with a polymeric toner pattern (Figure 3, step 3). Similar to the production of printed circuit boards, the exposed metal (the toner serves as resistant) is etched off in an iron chloride solution, resulting in the toner-coated copper line pattern (Figure 3, step 4). To finalize the flexible copper pattern, the remaining toner is removed by dissolving in acetone (Figure 3, step 5). To establish whether the copper line pattern did not suffer from this procedure, conductivity was measured by a multimeter. The connecting copper line shows a total length of 21 cm. Over a distance of 0.5 cm, a resistance of 0.2 Ω was measured, and over 21 cm the measurement revealed a value of 8.9 Ω. Assuming that the connecting line shows the same geometry over the whole distance, the increase in resistance can mainly be attributed to the increasing distance between the electrodes. Furthermore, we found that the mechanical stability of the flexible line pattern is very high. The relative deviation of the electrical resistance from the mean value calculated after 500 folding cycles was determined to be only 0.34 % (Supporting Information, Figure S3).

In summary, an electroless, liquid-phase deposition technique has been presented for the fabrication of two types of copper: freestanding thin copper foils and copper-plated Kapton. Copper films with high purity, dense microstructure, large grains, and consequently excellent electrical conductivity are formed, and the process is able to overcome the major limitations of present electroless deposition techniques. Furthermore, the low synthesis temperature makes it a cost-effective alternative to high-vacuum approaches for the production of high-end devices, such as thin and flexible capacitors, transparent conductive coatings, electrode material for battery applications, or flexible electronics, as exemplified herein by the conduction-line patterns obtained from copper-plated Kapton.

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